

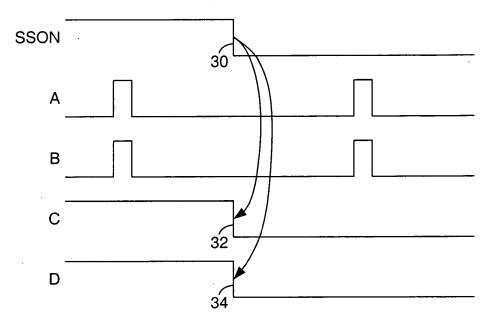
FIG. 1

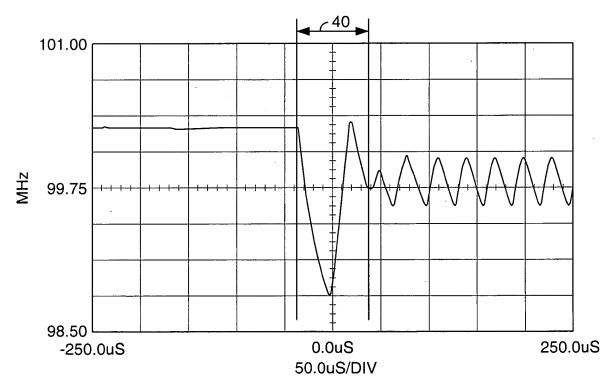
100 -114 REF 0 -112 SSON\_A -110 ر118 122 118 CLK 108 1157 CPU/ **FDBCK SYNCHRONIZER MODULATOR** SSONO **MOTHERBOARD** 416 126 106 SSON\_B 120 124-125-

FIG. 3

BEST AVAILABLE COPY

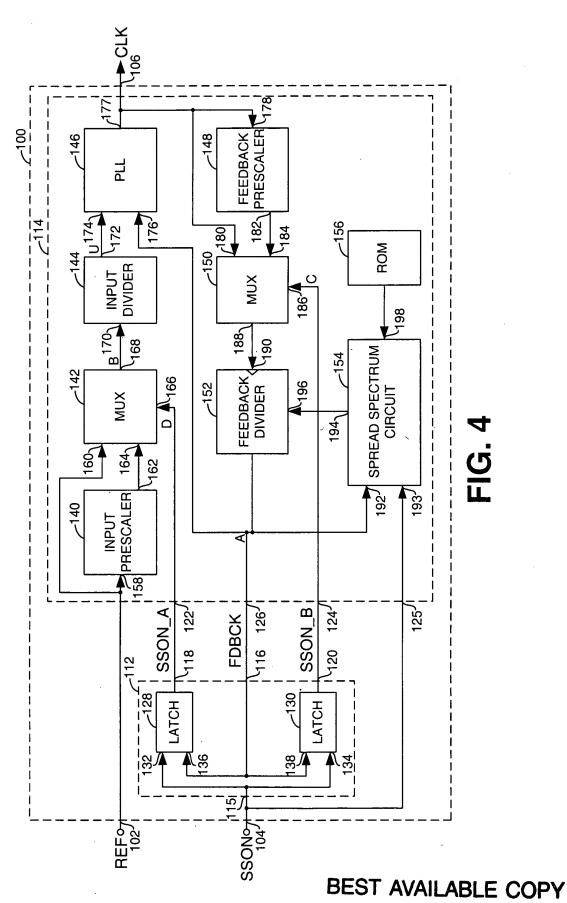






(CONVENTIONAL) FIG. 2







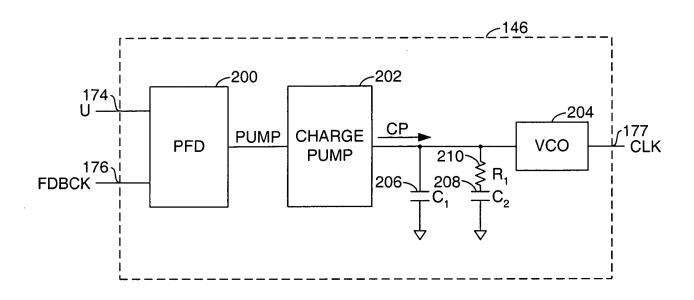
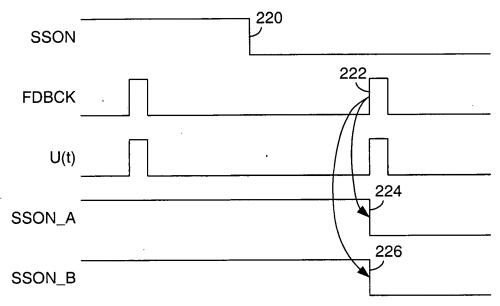


FIG. 5





## SPREAD SPECTRUM TRANSITION BEHAVIORS ARE CONTROLLED BY THE PROGRAM

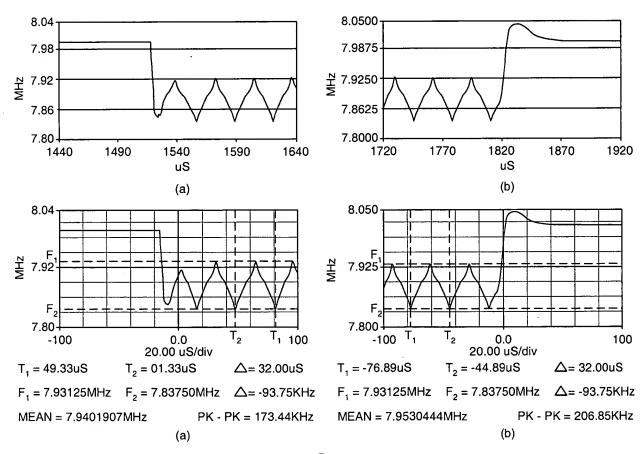
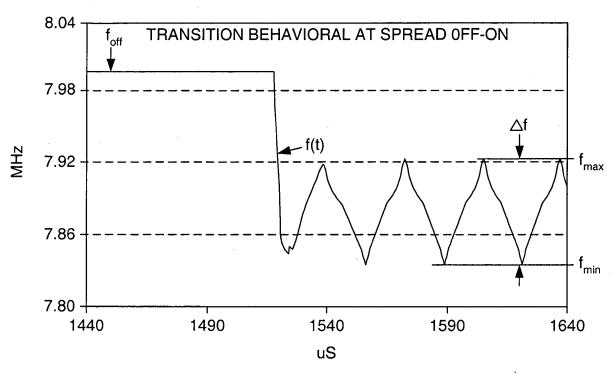


FIG. 6

## **BEST AVAILABLE COPY**



## CRITERIA FOR DETERMINING "GOOD AND BAD" SS TRANSIENT BEHAVIOR



f(t): PLL's RUNNING FREQUENCY IN TRANSIENT PERIOD

f<sub>off</sub>: PLL's SSCG OFF FREQUENCY

 $\mathbf{f}_{\text{max}}$ : MAXIMUM FREQUENCY IN SSCG ON

 $\mathbf{f}_{\min}$ : MINIMUM FREQUENCY IN SSCG ON

△f: PEAK TO PEAK FREQUENCY IN SSCG

CRITERIA NEED TO BE SATISFIED:

FREQUENCY RUNNING RANGE DURING TRANSIENT  $f_{min} \le f(t) \le f_{off}$ 

FIG. 7



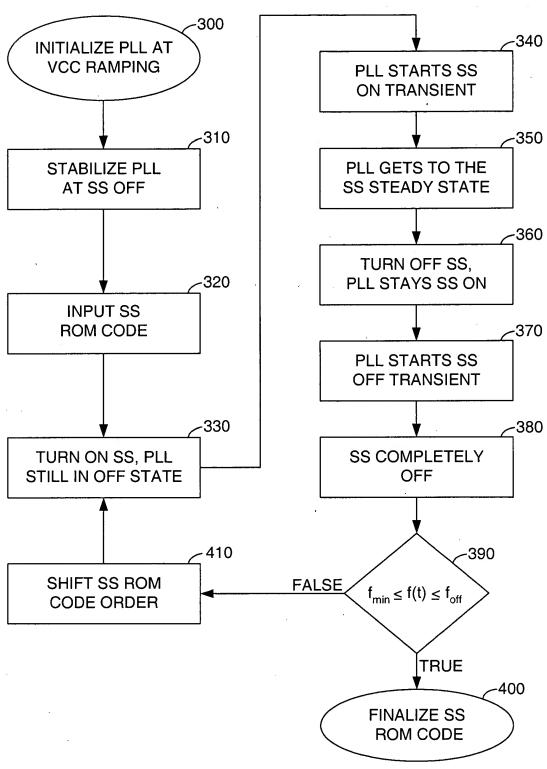
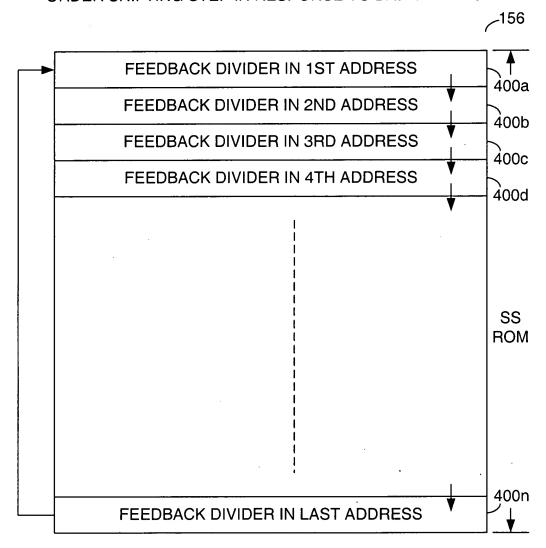


FIG. 8



## ORDER SHIFTING STEP IN RESPONSE TO BAD BEHAVIOR



MOVE FEEDBACK DIVIDER IN LAST ADDRESS TO 1ST ADDRESS AND SHIFT DOWN SS ROM CODE.

FIG. 9